Amendments to the Claims:

The following Listing of Claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1. (Currently Amended) A method for sealing a thin film transistor comprising the steps of:

(a) providing a thin film transistor comprising a gate electrode, a gate dielectric, a source and a drain electrode, and a semiconductor layer; and

(b) vapor depositing a sealing material on at least a portion of said semiconductor layer through a pattern of ~~an~~ a polymeric aperture mask,

wherein said aperture mask is reusable and repositionable.

2. (Currently Amended) The method of claim 1 wherein said sealing material forms a ~~preselected~~ pattern on at least a portion of said semiconductor layer, and the pattern formed by said sealing material is the pattern of the aperture mask.

3. (Original) The method of claim 1 wherein said sealing material has a resistivity of at least 10x that of said semiconductor layer.

4. (Original) The method of claim 1 wherein said sealing material has a resistivity of at least 100x that of said semiconductor layer.

5. (Original) The method of claim 1 wherein said sealing material has a resistivity of at least $1x10^6$ ohm-cm.

6. (Original) The method of claim 1 wherein said sealing material is a metal oxide, metal nitride, silicon oxide, silicon nitride, or a polymer.

7. (Currently Amended) The method of claim 6 wherein said sealing material is a polymer, and said polymer is parylene.

8. (Original) The method of claim 1 wherein said sealing material is transparent.

9. (Original) The method of claim 1 wherein said semiconductor layer is an organic semiconductor.

10. (Original) The method of claim 9 wherein said organic semiconductor comprises pentacene or a substituted pentacene.

11. (Currently Amended) The method of claim 1 wherein said aperture mask comprises ~~is~~ a polymeric film, said pattern is formed through said polymeric film, and said polymeric film is reusable and repositionable ~~aperture mask~~.

12. (Withdrawn) The method of claim 9 wherein said thin film transistor further comprises a surface treatment layer interposed between said dielectric layer and said semiconductor layer.

13. (Currently Amended) The method of claim 1 further comprising ~~the step of~~ vapor depositing a metal layer on said sealing material through said pattern of said aperture mask.

14. (Currently Amended) The method of claim 1 further comprising ~~the step of~~ interconnecting said thin film transistor to at least one other thin film transistor to form an integrated circuit.

15. (Currently Amended) A method of making an integrated circuit comprising the ~~The~~ method of claim 1, wherein said integrated circuit comprises said thin film transistor ~~is part of an the integrated circuit~~ and at least one other component.

16. (Currently Amended) The method of claim 15 wherein said sealing material covers at least a portion of said integrated circuit other said thin film transistor.

17. (Currently Amended) The method of claim 16 wherein said integrated circuit comprises conducting lines, and said sealing material covers at least a portion of said conducting lines ~~of said integrated circuit~~.

18. (Currently Amended) A method of making a thin film transistor comprising the steps of:

(a) providing a substrate;

(b) depositing a gate electrode material on said substrate through a first aperture mask pattern ~~of an aperture mask~~;

(c) depositing a gate dielectric on said gate electrode material through a second aperture mask pattern ~~of an aperture mask~~;

(d) depositing a semiconductor layer adjacent to said gate dielectric through a third aperture mask pattern ~~of an aperture mask~~;

(e) depositing a source electrode and a drain electrode contiguous to said semiconductor layer through a fourth aperture mask pattern ~~of an aperture mask~~; and

(f) vapor depositing a sealing material on at least a portion of said semiconductor layer through a fifth aperture mask pattern of ~~an~~ a polymeric aperture mask,

wherein said polymeric aperture mask is reusable and repositionable.

19. (Original) The method of claim 18 wherein at least one of said depositing steps (b) to (e) are vapor depositing steps under vacuum.

20. (Original) The method of claim 19 wherein all of said depositing steps (b) to (e) are vapor depositing steps under vacuum.

21. (Currently Amended) The method of claim 20 wherein all of said depositing steps (b) to (f) are ~~the method is~~ carried out ~~in its entirety~~ without breaking vacuum.

22. (Currently Amended) The method of claim 18 wherein the steps (a) through (f) are performed in the order listed.

23. (Original) The method of claim 18 wherein said sealing material has a resistivity of at least 10x that of said semiconductor layer.

24. (Original) The method of claim 23 wherein said sealing material is transparent.

25. (Original) The method of claim 18 wherein said semiconductor layer is an organic semiconductor.

26. (Original) The method of claim 25 wherein said organic semiconductor layer comprises pentacene or a substituted pentacene.

27. (Currently Amended) The method of claim 18 wherein said gate electrode material, gate dielectric, semiconductor layer, source and drain electrodes, and sealing material are deposited through a single aperture mask formed with each said aperture mask pattern ~~a pattern of deposition apertures~~.

28. (Original) The method of claim 18 wherein said gate electrode material, gate dielectric, semiconductor layer, source and drain electrodes, and sealing material are each deposited through a separate aperture mask of a mask set.

29. (Withdrawn) The method of claim 18 further comprising the step of depositing a surface treatment layer between said dielectric layer and said semiconductor layer.

30. (Withdrawn) A transistor comprising a substrate, a gate electrode, a gate dielectric, a source and drain electrode, a semiconductor layer, and a vapor deposited sealing

layer on at least a portion of said semiconductor layer.

31. (New) The method of claim 18 wherein said polymeric aperture mask comprises a polymeric film, said fifth aperture mask pattern is formed through said polymeric film, and said polymeric film is reusable and repositionable.

32. (New) The method of claim 11 wherein said polymeric film has a thickness of less than 200 microns.

33. (New) The method of claim 11 wherein said polymeric film has a thickness in the range of from about 5 microns to about 50 microns.

34. (New) The method of claim 11 wherein said polymeric film is a polyimide film.